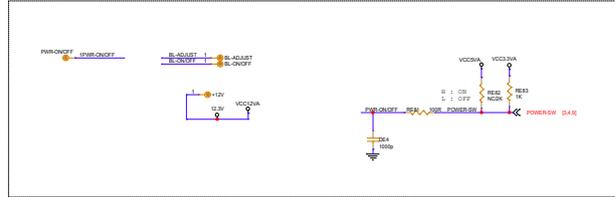
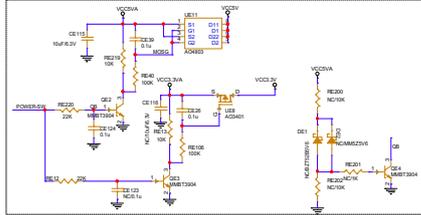


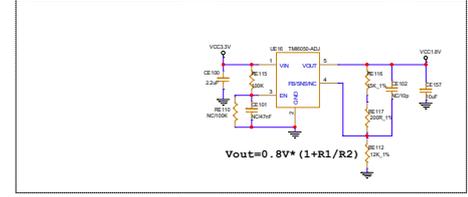
+12V Input



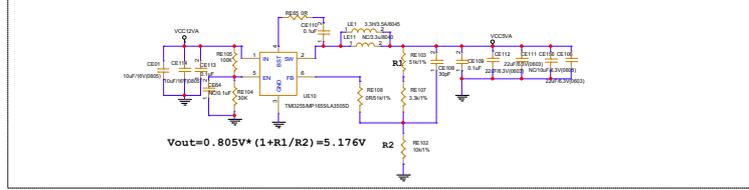
+3.3V Normal Power +5V Normal Power



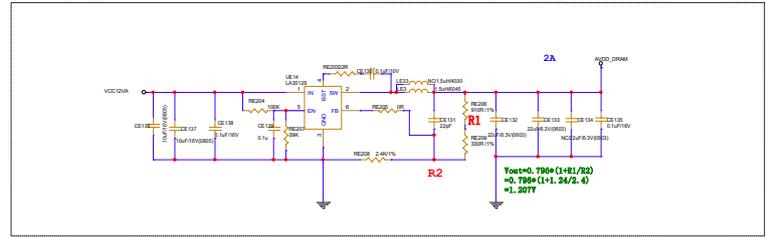
+1.8V Normal Power



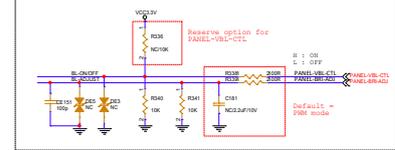
+5V Standby Power



+1.2V Standby Power

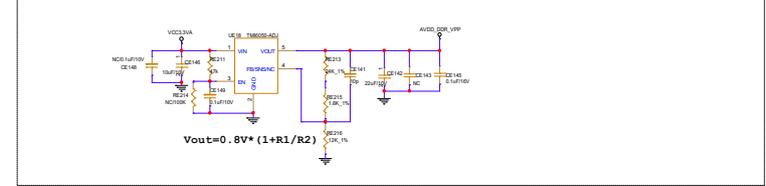


Backlight

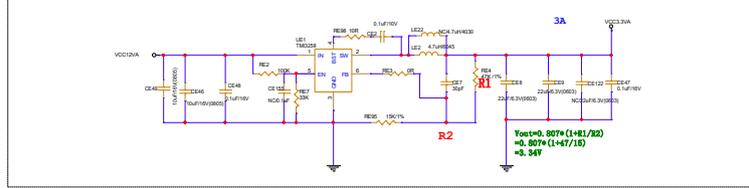


BLON BLON/OFF  
 PWRON PWRON/OFF

+2.5V Standby Power

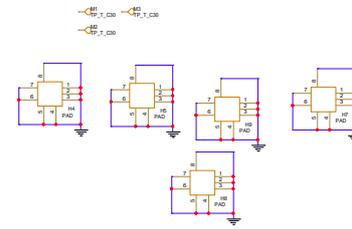
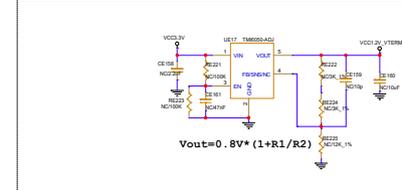


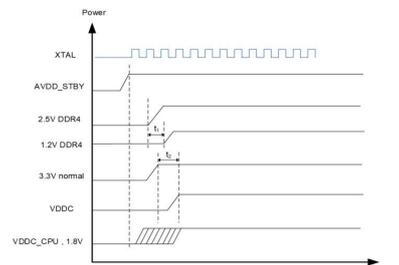
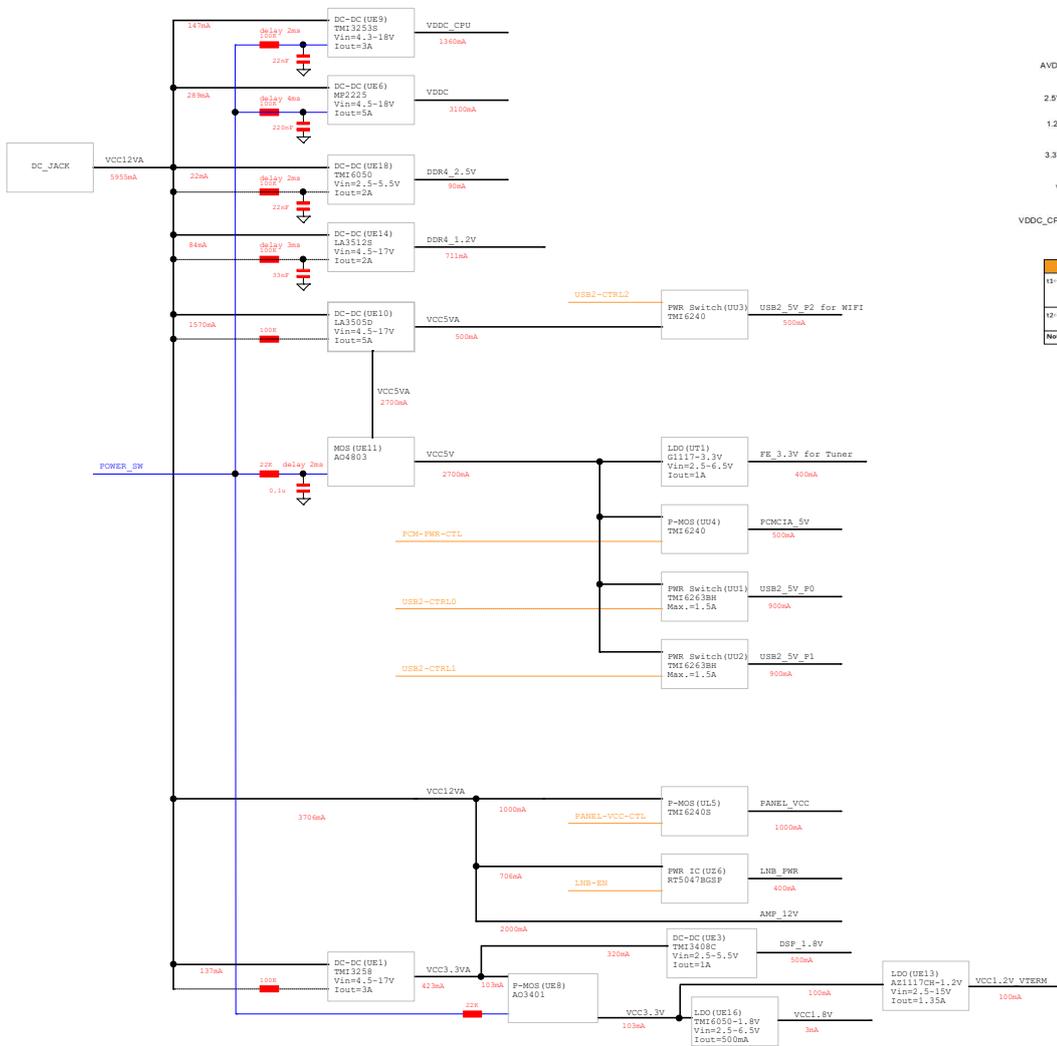
+3.3V Standby Power



+1.2V CML VTERM Power

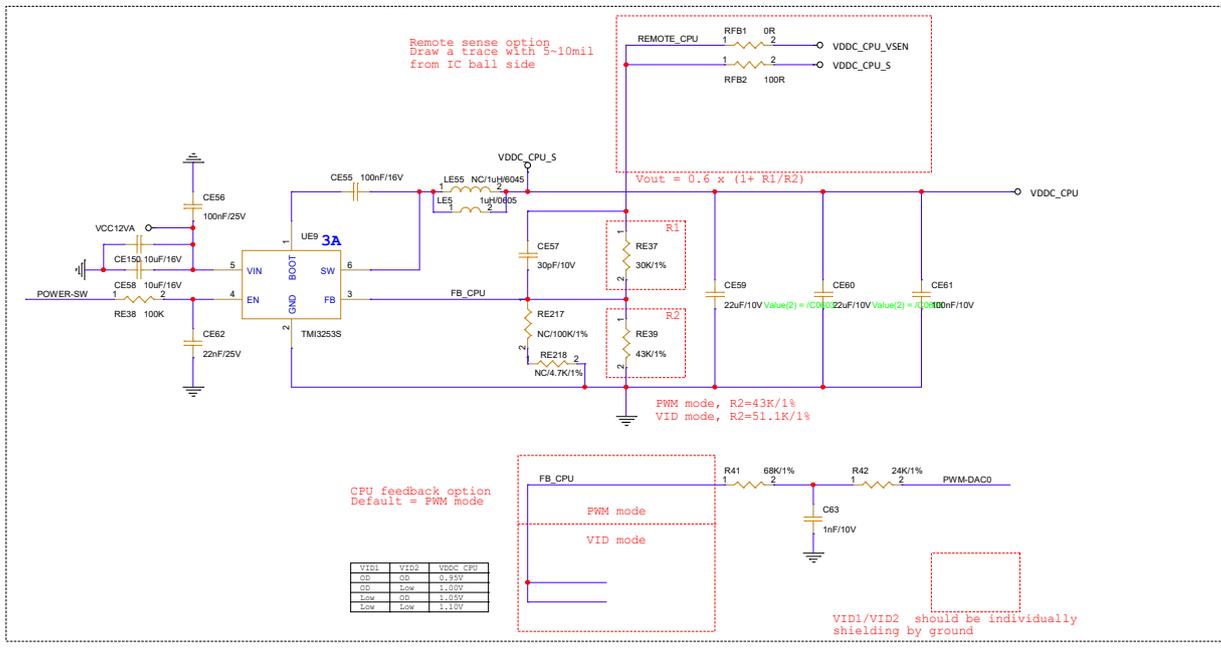
CML panel only, can remove following circuit for others



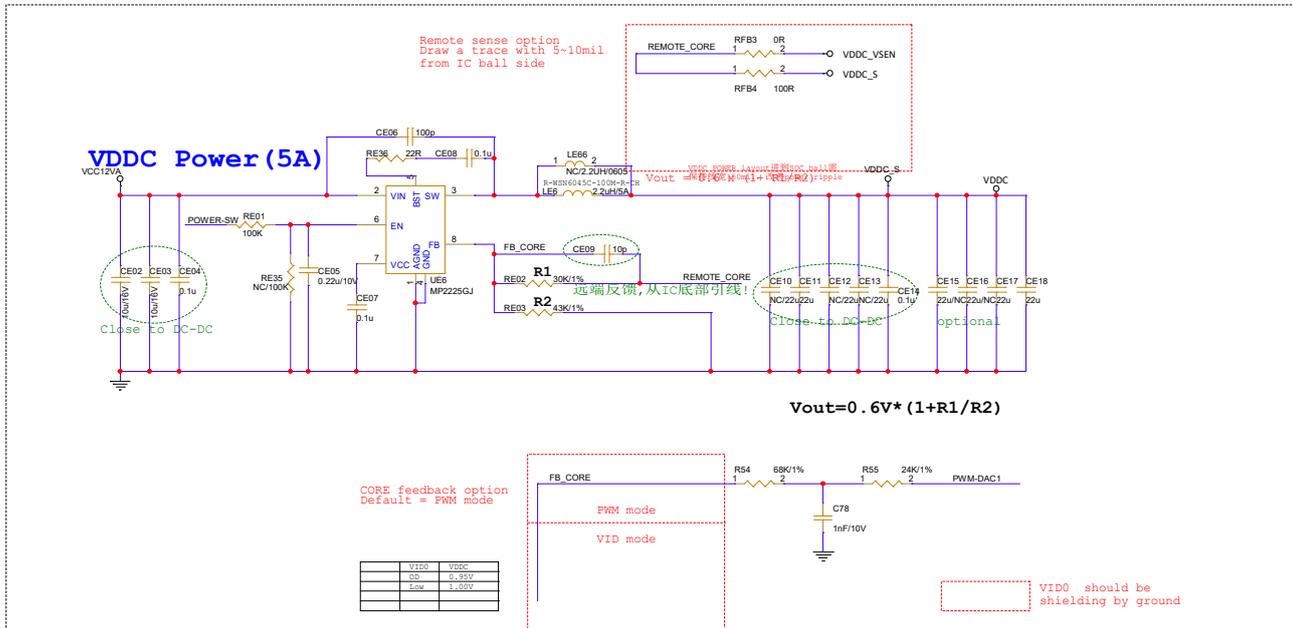


Time	Description	Min	Typ	Max	Unit
t1	2.5V must ramp at the same time or earlier than 1.2V and 2.5V must be equal to or higher than 1.2V at all times.	0	---	---	ns
t2	3.3V normal rising edge 100% to VDDC rising edge 100% lead time.	1	---	---	ns

Note: Keep AVDD\_STBY power ready earlier than other powers.

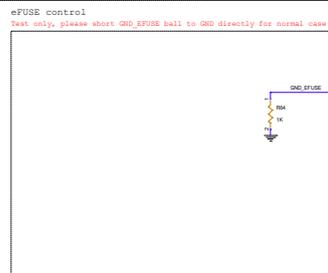
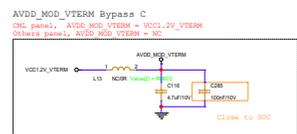
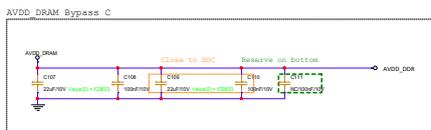
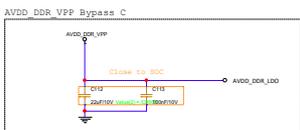
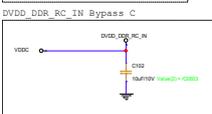
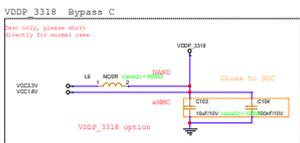
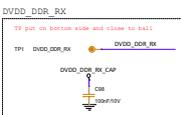
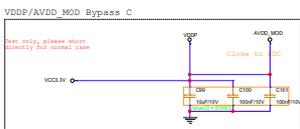
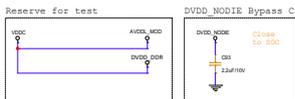
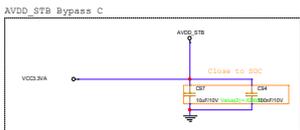


POWER-SW << POWER-SW [2,4,9]  
PWM-DAC0 << PWM-DAC0 [9]

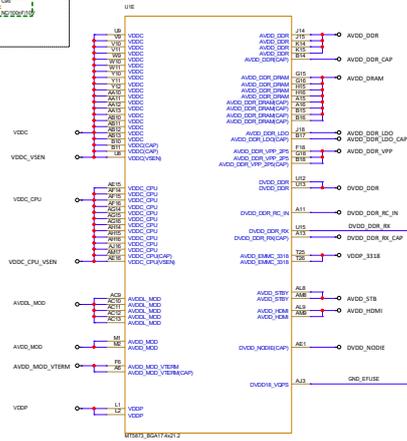
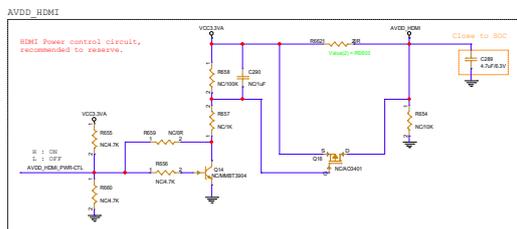
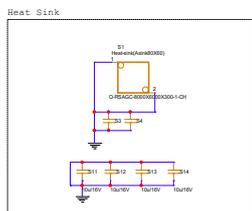


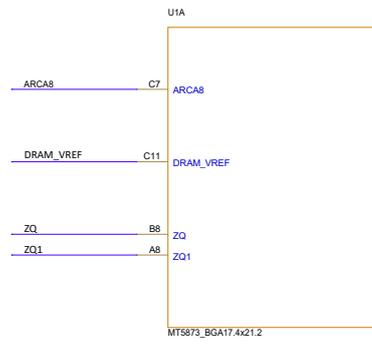
POWER-SW << POWER-SW [2,3,9]

PWM-DAC1 << PWM-DAC1 [9]

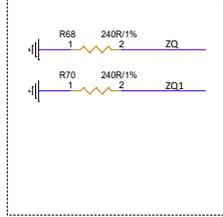


AVDD\_HDMI\_PWR\_CTL

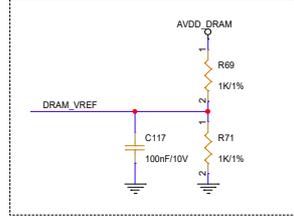




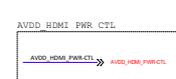
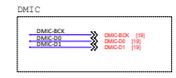
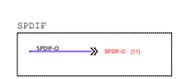
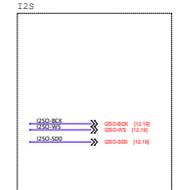
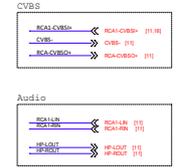
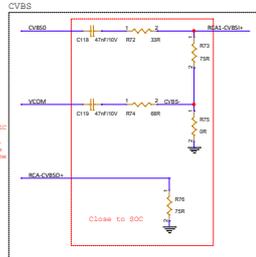
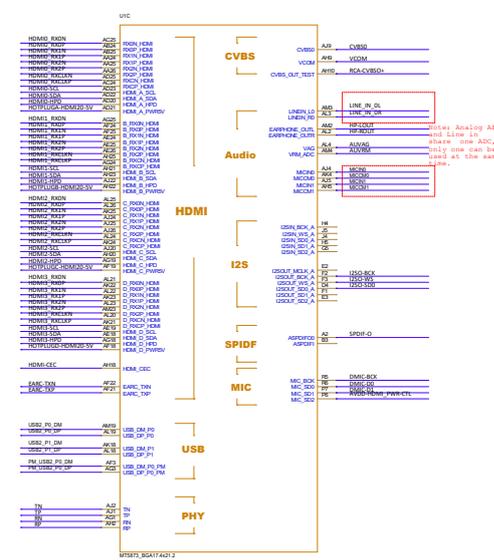
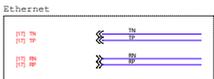
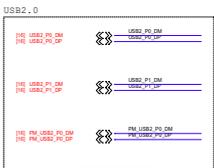
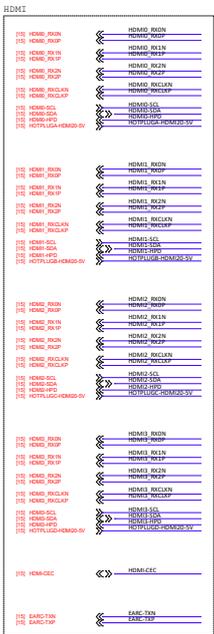
MCP DRAM ZQ Resistor



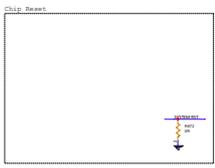
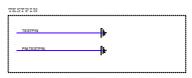
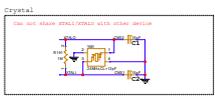
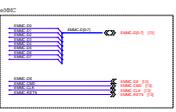
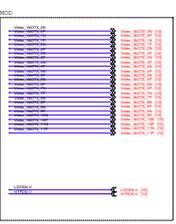
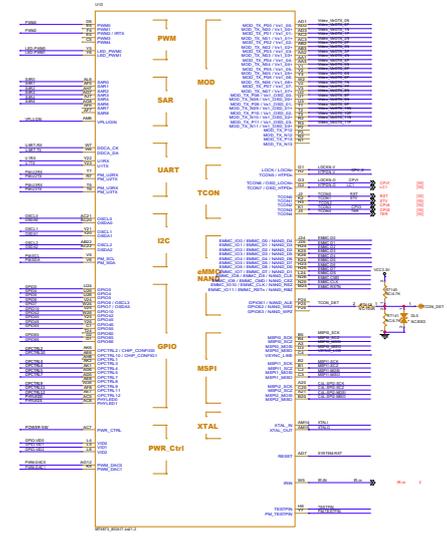
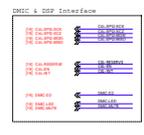
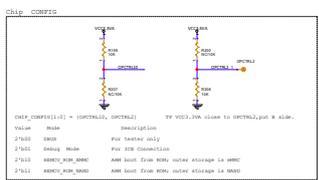
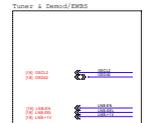
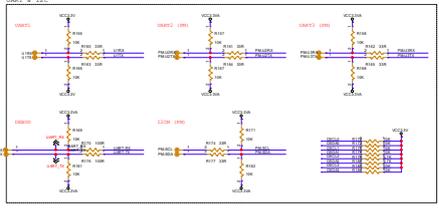
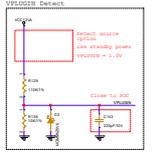
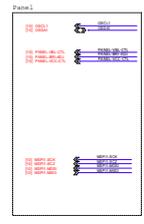
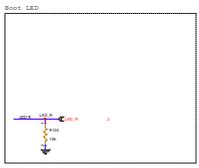
MCP DRAM VREF



<b>CHANGHONG</b> 长虹		<b>MT9603</b>	
Schematic Name		<b>MT9603 DRAM</b>	Rev <b>VER1.0</b>
Size <b>B</b>	Sheet <b>6 of 21</b>	Date: <b>Saturday, September 21, 2024</b>	

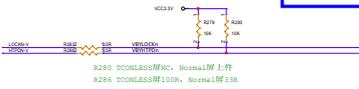
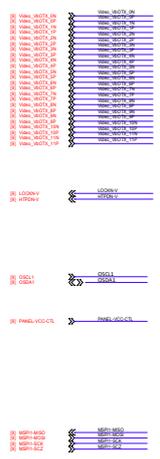




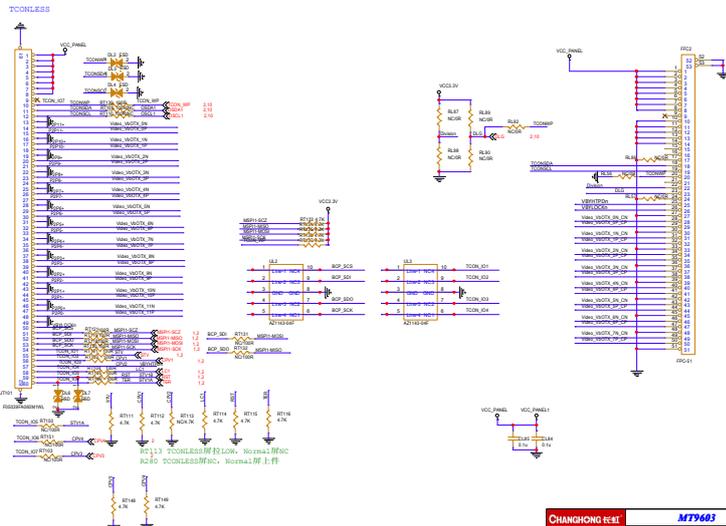
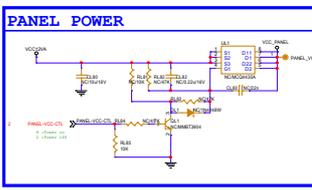
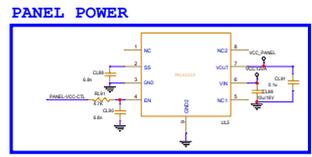


V1 = 100uF; Csbars = 0.8

Wm1.W0721_09	C01	100000000	Wm1.W0721_09_01
Wm1.W0721_09	C02	100000000	Wm1.W0721_09_02
Wm1.W0721_09	C03	100000000	Wm1.W0721_09_03
Wm1.W0721_09	C04	100000000	Wm1.W0721_09_04
Wm1.W0721_09	C05	100000000	Wm1.W0721_09_05
Wm1.W0721_09	C06	100000000	Wm1.W0721_09_06
Wm1.W0721_09	C07	100000000	Wm1.W0721_09_07
Wm1.W0721_09	C08	100000000	Wm1.W0721_09_08
Wm1.W0721_09	C09	100000000	Wm1.W0721_09_09
Wm1.W0721_09	C10	100000000	Wm1.W0721_09_10
Wm1.W0721_09	C11	100000000	Wm1.W0721_09_11
Wm1.W0721_09	C12	100000000	Wm1.W0721_09_12
Wm1.W0721_09	C13	100000000	Wm1.W0721_09_13
Wm1.W0721_09	C14	100000000	Wm1.W0721_09_14
Wm1.W0721_09	C15	100000000	Wm1.W0721_09_15
Wm1.W0721_09	C16	100000000	Wm1.W0721_09_16
Wm1.W0721_09	C17	100000000	Wm1.W0721_09_17
Wm1.W0721_09	C18	100000000	Wm1.W0721_09_18
Wm1.W0721_09	C19	100000000	Wm1.W0721_09_19
Wm1.W0721_09	C20	100000000	Wm1.W0721_09_20
Wm1.W0721_09	C21	100000000	Wm1.W0721_09_21
Wm1.W0721_09	C22	100000000	Wm1.W0721_09_22
Wm1.W0721_09	C23	100000000	Wm1.W0721_09_23
Wm1.W0721_09	C24	100000000	Wm1.W0721_09_24
Wm1.W0721_09	C25	100000000	Wm1.W0721_09_25
Wm1.W0721_09	C26	100000000	Wm1.W0721_09_26
Wm1.W0721_09	C27	100000000	Wm1.W0721_09_27
Wm1.W0721_09	C28	100000000	Wm1.W0721_09_28
Wm1.W0721_09	C29	100000000	Wm1.W0721_09_29
Wm1.W0721_09	C30	100000000	Wm1.W0721_09_30
Wm1.W0721_09	C31	100000000	Wm1.W0721_09_31
Wm1.W0721_09	C32	100000000	Wm1.W0721_09_32
Wm1.W0721_09	C33	100000000	Wm1.W0721_09_33
Wm1.W0721_09	C34	100000000	Wm1.W0721_09_34
Wm1.W0721_09	C35	100000000	Wm1.W0721_09_35
Wm1.W0721_09	C36	100000000	Wm1.W0721_09_36
Wm1.W0721_09	C37	100000000	Wm1.W0721_09_37
Wm1.W0721_09	C38	100000000	Wm1.W0721_09_38
Wm1.W0721_09	C39	100000000	Wm1.W0721_09_39
Wm1.W0721_09	C40	100000000	Wm1.W0721_09_40
Wm1.W0721_09	C41	100000000	Wm1.W0721_09_41
Wm1.W0721_09	C42	100000000	Wm1.W0721_09_42
Wm1.W0721_09	C43	100000000	Wm1.W0721_09_43
Wm1.W0721_09	C44	100000000	Wm1.W0721_09_44
Wm1.W0721_09	C45	100000000	Wm1.W0721_09_45
Wm1.W0721_09	C46	100000000	Wm1.W0721_09_46
Wm1.W0721_09	C47	100000000	Wm1.W0721_09_47
Wm1.W0721_09	C48	100000000	Wm1.W0721_09_48
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Wm1.W0721_09	C50	100000000	Wm1.W0721_09_50

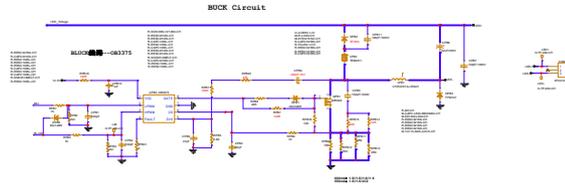
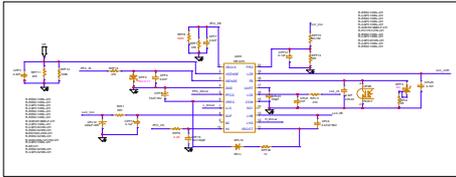
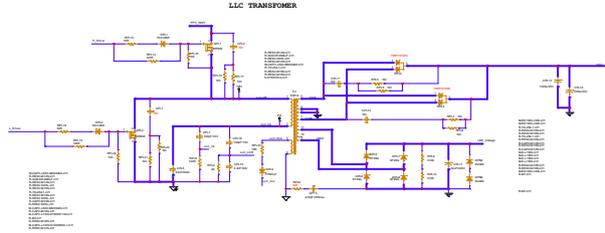
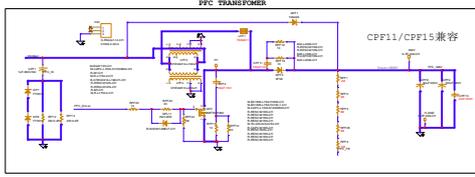
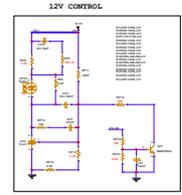
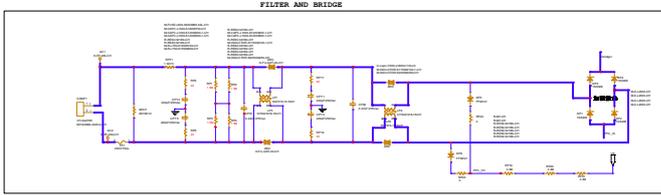


R280 TCONLESS#100, Normal屏上件  
R286 TCONLESS#100R, Normal屏上件

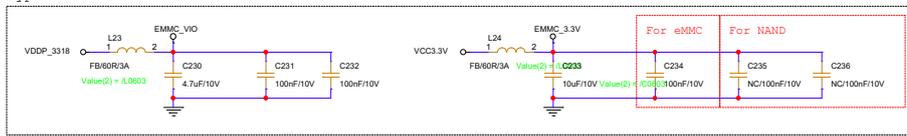




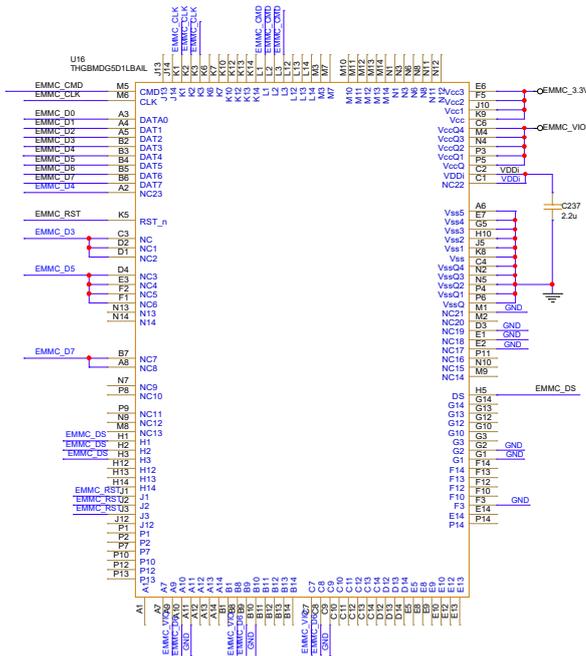
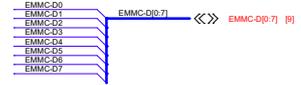
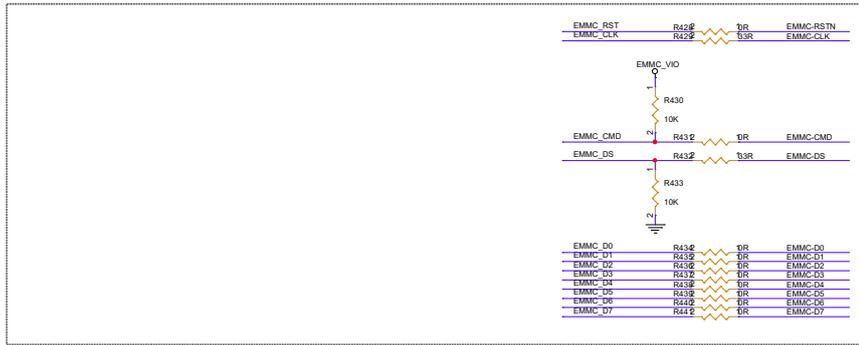




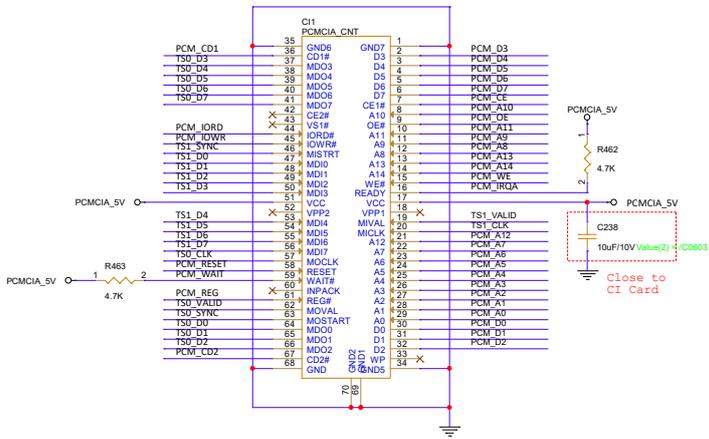
Bypass C



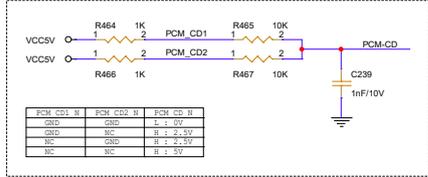
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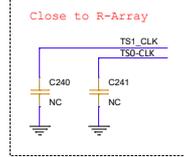
CHANGHONG 长虹		MT9603	
Schematic Name		Rev	
eMMC		VER1.0	
Sign	Sheet	Date:	
Custom	13 of 21	Saturday, September 21, 2024	



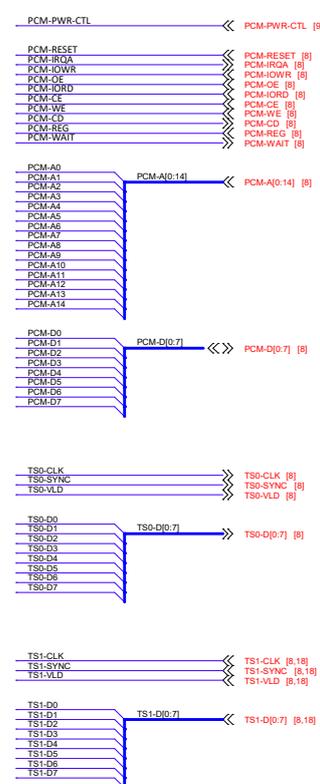
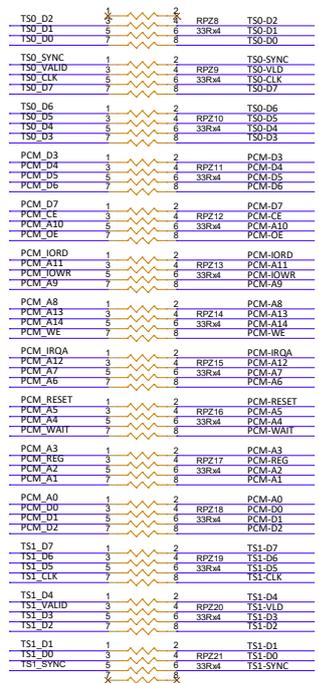
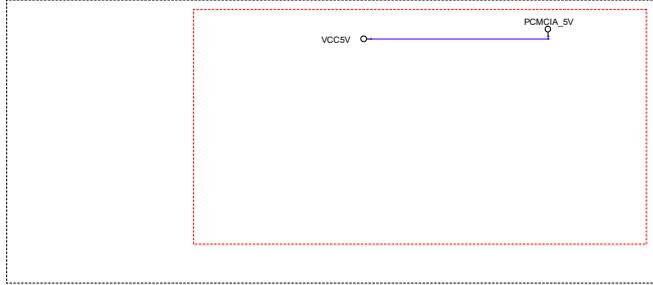
**PCMCIA Card Detect**



**For EMI**



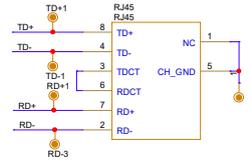
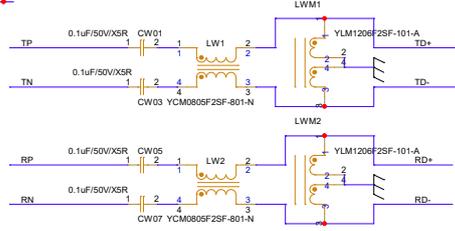
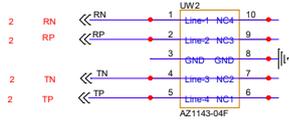
**PCMCIA Power Control**







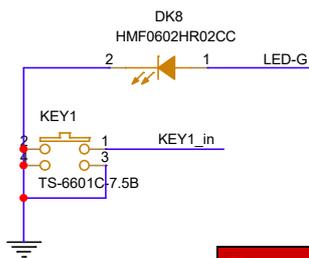
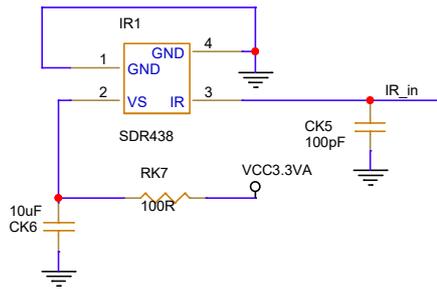
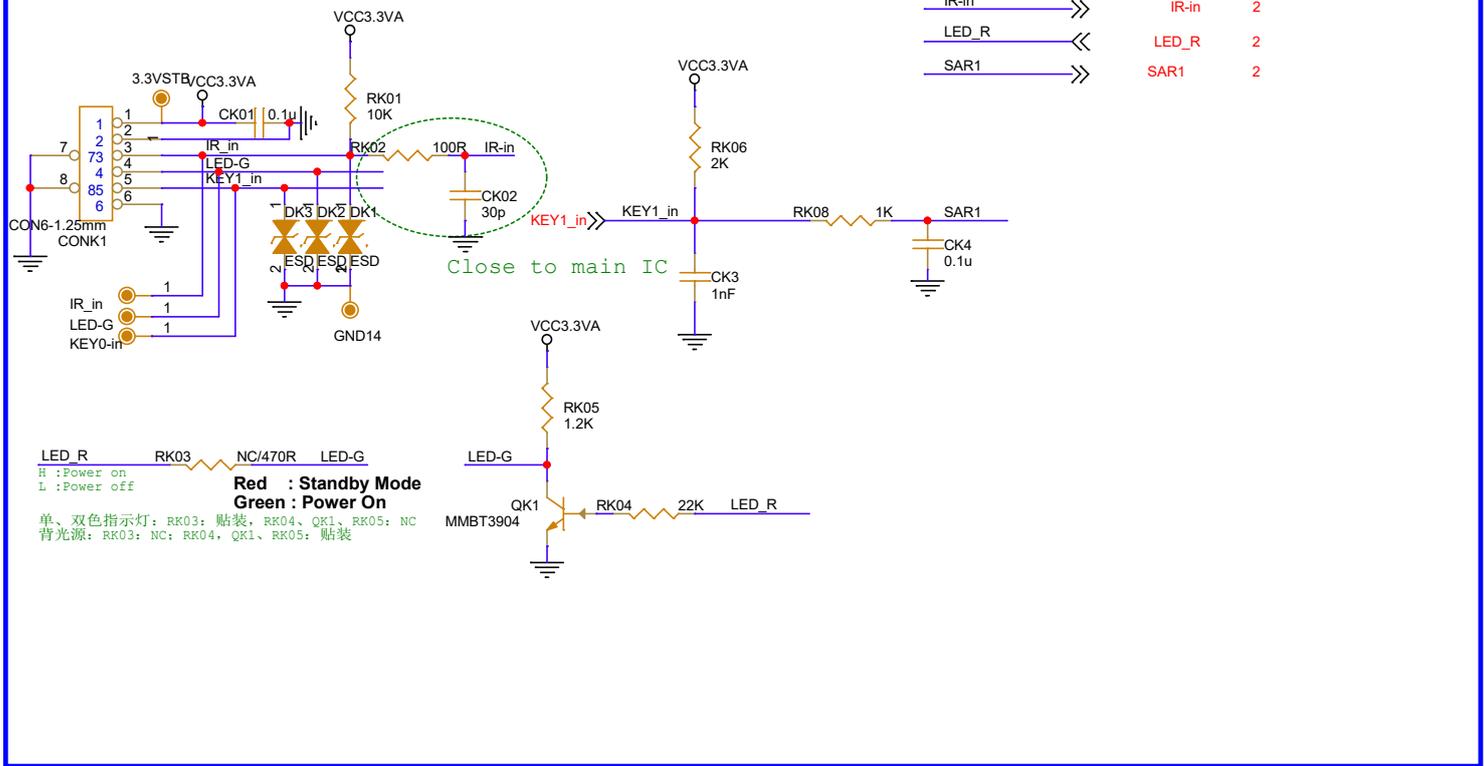
# LAN Interface



<b>CHANGHONG</b>		<b>MT9603</b>	
Schematic Name		Ethernet PHY	
Rev		VER1.0	
Size	Sheet	Date:	Tuesday, November 12, 2024
Custom	17 of 21		



# IR & KEY



<b>CHANGHONG 长虹</b>		<b>MT9603</b>	
Schematic Name		<b>KEY &amp; IR &amp; LS</b>	Rev <b>VER1.0</b>
Size Custom	Sheet 19 of 21	Date:	Wednesday, January 15, 2025